AMENDMENTS TO THE CLAIMS

Cancel claims 8-10 without prejudice. Please accept amended claims 1, 11 and 14, and new claims 16-20 as follows:

1. (Currently Amended) An integrated circuit device comprising:

a pin for receiving a direct current voltage ~~component~~ signal;~~, the device comprising:~~

a signal source for applying an alternating current voltage signal to the pin;

a buffer for converting the alternating current voltage signal into a digital signal; and

a digital detector for detecting a frequency of the digital signal and outputting a predetermined detection signal.

2. (Original) The device of claim 1, wherein the predetermined detection signal is activated when the frequency of the digital signal is greater than or equal to a predetermined frequency.

3. (Original) The device of claim 2, wherein the digital detector comprises a transistor for attenuating a component of the digital signal having a predetermined logic level when the digital signal is oscillated at a frequency greater than or equal to a predetermined frequency.

4. (Original) The device of claim 2, wherein the predetermined detection signal is a signal for setting predetermined functional modes.

5. (Original) The device of claim 1, further comprising:

a register chain for generating successive transfer signals according to the digital signal in response to a clock signal; and

a decoder for generating functional mode signals according to transfer signals in response to the predetermined detection signal.

6. (Original) The device of claim 5, wherein the register chain comprises registers for generating the transfer signals.

7. (Original) The device of claim 5, wherein the decoder generates the functional mode signals through a logical combination of the transfer signals.

8-10. (Cancelled)

11. (Currently Amended) The device of claim ~~10~~ 1, wherein the digital detector comprises a plurality of inverter stages responsive to a reference signal.

12. (Original) The device of claim 11, wherein each inverter stage comprises:

a PMOS transistor; and

an NMOS transistor coupled in series to the PMOS transistor, the NMOS transistor having a size smaller than a size of the PMOS transistor.

13. (Original) The device of claim 12, wherein the functional mode signal depends on the size of the NMOS transistor for pull-down.

14. (Currently Amended) The device of claim ~~10~~ 1, wherein the functional mode signal is activated when the frequency of the digital signal is greater than a predetermined minimum frequency.

15. (Original) The device of claim 14, wherein the predetermined minimum frequency depends on a size of an NMOS transistor relative to a PMOS transistor in an inverter stage of the digital detector.

16. (New) An integrated circuit device comprising a pin for receiving a direct current voltage signal, the device comprising:

a signal source for applying an alternating current voltage signal to the pin;

a buffer for converting the alternating current voltage signal into a digital signal; and

a digital detector for detecting a frequency of the digital signal and outputting a predetermined detection signal;

a register chain for generating successive transfer signals according to the digital signal in response to a clock signal; and

a decoder for generating functional mode signals according to transfer signals in response to the predetermined detection signal.

17. (New) An integrated circuit device comprising a pin for receiving a direct current voltage signal, the device comprising:

a signal source for applying an alternating current voltage signal to the pin;

a buffer for converting the alternating current voltage signal into a digital signal; and

a digital detector for detecting a frequency of the digital signal and outputting a predetermined detection signal, wherein the digital detector comprises a plurality of inverter stages responsive to a reference signal.

18. (New) The device of claim 17, wherein each inverter stage comprises:

a PMOS transistor; and

an NMOS transistor coupled in series to the PMOS transistor, the NMOS transistor having a size smaller than a size of the PMOS transistor.

19. (New) The device of claim 18, wherein the functional mode signal depends on the size of the NMOS transistor for pull-down.